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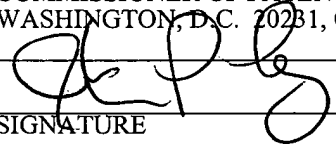
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Pozder
Serial No.: 09/443,443
Filed: November 22, 1999
For: METHOD FOR FORMING
A SEMICONDUCTOR DEVICE
HAVING A MECHANICALLY
ROBUST PAD INTERFACE

October 25, 2002

Art Unit: 7259
Examiner: M. Estrada
Docket No.: SC10861TP

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APPELLANTS' BRIEF ON APPEAL

HONORABLE COMMISSIONER OF PATENTS AND TRADEMARKS
WASHINGTON, D.C. 20231

BOARD OF PATENT APPEALS & INTERFERENCES:

This brief is filed pursuant to 37 C.F.R. §1.192 in the matter of the Appeal to the Board of Appeals and Interferences of the rejection of the claims of the above-referenced application for patent. A Petition extending the response period is submitted herewith. A check for fees is enclosed. If, however, the check is lost or insufficient, please debit the insufficiency or credit any refund to Deposit Account 13-4773. This page is enclosed in triplicate for this purpose.

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REAL PARTY IN INTEREST

The present application is wholly assigned to MOTOROLA, INC., a Delaware corporation with its headquarters in Schaumburg, Illinois.

RELATED APPEALS AND INTERFERENCES

Appellants are unaware of other appeals or interferences which will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claim 1-23 were submitted with the original application and claims 24-32 were added subsequently.

Claims 7 and 12-23 are cancelled.

Claims 1-5, 10, 24-27, 30 and 32 stand rejected under 35 USC § 103(a) as being unpatentable over the combination of Freeman, Jr. et al., United States Patent No. 5,149,674, hereinafter "Freeman", and Lien, United States Patent No. 5,989,991, hereinafter "Lien".

Claim 6 stands rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Freeman and Lien as applied to claims 1-5, 10, 24-27, 30 and 32 above, and further in view of Takiar et al., United States Patent No. 4,723,197, hereinafter "Takiar".

Claims 8, 9, 28-29 and 31 stand rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Freeman and Lien as applied to claims 1-5, 10, 24-27, 30 and 32 above, and further in view of White, United States Patent No. 5,942,448, hereinafter "White".

Claim 11 stands rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Freeman and Lien as applied to claims 1-5, 10, 24-27, 30 and 32 above, and further in view of Hwang et al., United States Patent No. 5,912,510, hereinafter "Hwang".

The claims being appealed are 1, 8, 24, and 32, as amended or added in Appellants' communication mailed November 1, 2001; claims 25-31 as amended or added in Appellants communication mailed May 14, 2001; claims 2-6 as amended in Appellants' communication mailed March 28, 2001; and claims 9-11 as originally filed.

STATUS OF AMENDMENTS

No amendments were filed subsequent to final rejection.

SUMMARY OF THE INVENTION

Appellants' invention relates generally to a process for forming semiconductor devices having mechanically robust bond pad interfaces. Integrated circuits typically include bond pads that provide the means for transferring electrical signals and power from and to the die via probe needles, bonding wires, conductive bumps, and the like. Bond pads may include aluminum, copper, or alloys thereof. Although copper has electrical properties superior to those of aluminum, copper is a non-self-passivating metal and oxidation or corrosion of copper bond pads can occur when the die is exposed to the atmosphere. Aluminum is self-passivating and, therefore, more resistant to degradation from atmospheric exposure. To realize the advantages of the self-passivating character of aluminum and the superior electrical characteristics of copper, composite bond pad structures, in which an underlying layer of copper interfaces with other layers in the integrated circuit while a corrosion-resistant aluminum capping layer is

formed on top of the copper. A thin barrier layer may be included intermediate between the copper and aluminum.

Conventional composite bond pads can exhibit poor mechanical properties, especially when the pads are probed by needles or other elements used to contact the pads. These poor mechanical properties can result in the formation of undesirable intermetallics at interfaces damaged by probe needles and the propagation to lower device layers of physical forces caused by probe needles and other elements.

Appellants' invention provides a composite bond pad that is resistant to external forces which may be applied during post-fabrication operations that utilize the bond pads. The composite bond pad includes a non-self-passivating conductive bond pad that is formed over a semiconductor substrate. A dielectric layer is then formed over the conductive bond pad. Portions of the dielectric layer are removed such that the dielectric layer becomes perforated and a portion of the conductive bond pad is exposed. Remaining portions of the dielectric layer form support structures that overlie that bond pad. A self-passivating conductive capping layer is then formed overlying the bond pad structure, where the perforations in the dielectric layer allow for electrical contact between the capping layer and the exposed portions of the underlying bond pad. The support structures provide a mechanical barrier that protects the interface between the capping layer and the bond pad.

A discussion of one embodiment of the invention begins on page 9, line 3 of the present application. A dielectric (passivation) layer 136 is formed over an uppermost interconnect level 133 and a conductive bond pad 134. Portions of dielectric layer 136 are removed to form a perforated

region within the dielectric layer that includes a plurality of support structures 138. The perforated region overlies conductive bond pad 134 such that a portion of the conductive bond pad 134 is exposed. At least some of the support structures 138 may remain connected to dielectric layer 136.

As depicted in FIG. 2, a barrier layer 202, which may include tantalum, titanium, tungsten, chromium, or the nitrides of these materials is formed within the perforated region of dielectric layer 136. A conductive capping layer 204 is then formed over support structures 138. Conductive capping layer 204 typically includes a self-passivating material such as aluminum.

The perforations in the dielectric layer 136 permit electrical contact between the self-passivating material that makes up the capping layer 204 and the conductive bond pad 134. Simultaneously, support structures 138 provide mechanical shielding of the interface between capping layer 204 and conductive bond pad 134. Additional mechanical shielding is achieved if some of support structures 138 are interconnected with unremoved portions of dielectric layer 136 because external forces applied to capping layer 204 will be distributed across dielectric layer 136.

ISSUES

- 1) Are claims 1-4, 6, 10, 11, 24-26, and 32 patentable over Freeman in view of Lien under 35 U.S.C. 103(a)?
- 2) Are claims 5 and 27 patentable over Freeman in view of Lien under 35 U.S.C. 103(a)?
- 3) Are claims 8, 9, 28, 29, and 31 patentable over Freeman in view of Lien and White under 35 U.S.C. 103(a)?

4) Is claim 30 patentable over Freeman in view of Lien under 35 U.S.C. 103(a)?

GROUPING OF CLAIMS

The Appellants respectfully request that the appealed claims be considered according to the following division:

Group A--> Claims 1-4, 6, 10, 11, 24-26, and 32

Group B--> Claims 5 and 27

Group C--> Claims 8, 9, 28, 29, and 31

Group D--> Claim 30

The requested division is on the basis that the claims of Group A are directed to a method of forming a composite bond pad structure in which a perforated passivation layer is formed between the formation of a first layer and a capping layer of the composite bond pad structure. The claims in Group B recite embodiments in which the support structures within the perforated passivation layer are connected to un-perforated (unremoved) portions of the layer. The claims in Group C include the a barrier layer between the first and capping layers of the composite bond pad structure. The claim in Group D is directed to an embodiment of the composite bond pad structure in which the first layer is copper and the capping layer is aluminum. Appellants submit that the claims of each group stand or fall together.

ARGUMENTS

Arguments Common to Groups A , B, C, and D

The Examiner uses Freeman and Lien in the rejections of claim Groups A, B, C, and D under 35 U.S.C. 103(a). Appellants respectfully submit that the Examiner has failed to establish a prima facie case of obviousness, which is the burden of the USPTO when rejecting claims under 35 U.S.C. 103. *In re Reuter*, 651 F.2d 751, 210 USPQ 249 (CCPA 1981). The case of prima facie obviousness is not met because the

references cited by the Examiner in support of the rejection do not teach or suggest all of the claim limitations recited in the claims of Groups A, B, C, and D. *In re Royka*, 180 USPQ 580 (CCPA 1974); *In re Wilson*, 165 USPQ 494 (CCPA 1970); *In re Fine*, 5 USPQ2d 1596 (CAFC1988).

More specifically, Appellants submit that Freeman and Lien fail to teach or suggest the removal of portions (the perforation) of a passivation layer to expose portions of a bond pad and form a plurality of support structures overlying the bond pad surface. Freeman and Lien both teach conventional patterning of the passivation layer in which a single, large opening is formed over the bond pad. In Freeman, the passivation layer 28 is patterned to form a single opening exposing the underlying interconnect while in Lien the passivation layer 209 is likewise patterned to form a single, conventional opening over the bond pad.

The Examiner rejected analogous arguments during prosecution indicating that Appellant had failed to distinguish its passivation layer from the interlevel dielectrics of Freeman. Appellants would respectfully submit that the term "passivation layer" is well known in the field of semiconductor fabrication to refer to that dielectric or insulating layer overlying the uppermost interconnect layer that is used to provide mechanical protection to the underlying integrated circuit and a barrier that prevents impurities including moisture from attacking the integrated circuit.

It is a well known principle that claims terms must be given their accustomed, ordinary or dictionary meaning unless the available interpretation aids point to another meaning. See, e.g., *Gentex Corp. v. Donnelly Corp.*, 69 F.3d 527, 30, 36 USPQ2d 1667, 1669 (Fed. Cir. 1995). Moreover, it has been held that claims "speak to those skilled in the art." *Electro Medical Systems, S.A. v. Cooper Life Sciences, Inc.* 34 F.3d 1048, 1054, 32 USPQ2d 1017, 1021 (Fed. Cir. 1994). As more recently stated by the Federal Circuit in *Multiform Desiccants, Inc. v. Medzam, Ltd.* 133 F.3d 1473, 45 USPQ2d 1429 (Fed. Cir. 1998):

It is the person of ordinary skill in the field of the invention through whose eyes the claims are construed. Such person is deemed to read the words used in the patent documents with an understanding of their meaning in the field, and to have knowledge of any special meaning and usage in the field.

In the case at hand, the person of ordinary skill in the field of semiconductor fabrication would recognize and interpret the term "passivation layer" in Appellants' independent claims as referring to a layer distinct from the interlevel dielectric layers. In a leading text in the field, for example, one finds the following discussion: "Silicon nitride is highly suitable as a passivation layer because...it behaves as a nearly impervious barrier to diffusion (in particular, moisture and sodium)." S. Wolf, *Silicon Processing for the VLSI Era Volume 1 Process Technology* p. 191 (Lattice Press 1986). This passage makes clear that, for at least the last 17 years, "passivation layer" has been used as a term that distinguishes the referred to layer from other layers within an integrated circuit. Referring even to Webster's, the word "passivate" is defined as "to protect (as a solid-state device) against contamination by coating or surface treatment." *Webster's Ninth New College Dictionary* (Merriam-Webster 1986). Thus, even non-technical sources support an interpretation of the passivation layer recited in Appellants' claims that would distinguish the recited element from perforated interlevel dielectric layer of Freeman.

Moreover, the perforated interlevel dielectric of Freeman does not suggest a perforated passivation layer as recited by Appellants because the purpose of perforating the dielectric layer in Freeman is to achieve greater planarity in a multi-layer bond pad structure. (Freeman - Abstract). Perforating the dielectric layer would have no effect on the planarity of the underlying bond pad structure and, accordingly, Freeman provides no motivation or suggestion to engage in such perforation. To the contrary, a perforated passivation layer in Freeman or Lien would have a serious technical drawback in that it would reduce the size of the "probable" area of the bond pad and lead to possible discontinuities. This is because neither

of the cited references disclose or suggest any the deposition of a conductive capping layer over the perforated bond pad as recited in Appellants claims.

In summary, because the pending independent claims 1, 24, and 32 each recite the removal of portions of a passivation layer to form support structures over the bond pad, Appellants submit that the references cited by the Examiner fail to disclose or suggest a limitation of the claimed invention and that, therefore, a prima facie case of obviousness has not been established and the rejection of the independent claims under 35 USC § 103(a) is improper. Because claims dependent upon a non-obvious claim are themselves non-obvious, Appellants would further submit that the Section 103(a) rejections of the pending dependent claims is also improper. Appellants respectfully request reversal of the claims in Groups A, B, C, and D.

Additional Arguments for Group B

In addition to the Arguments presented above, Appellants believe the claims of Group B are non-obvious over the cited references. The claims in Group B recite that the support structures are interconnected with the un-removed portions of the passivation layer. Neglecting, for the sake of argument, the distinction between the perforated dielectric of Freeman and Appellants' perforated passivation layer, Applicant would respectfully submit that the cited references still fail to disclose or suggest the support structure of Appellants' where the support structure is connected to un-removed portions of the dielectric layer. Referring to the Freeman figure, for example, it is clear that each of the structures that would correspond to the support structure of Appellants' is a free-floating structure that is not connected to the un-removed portions of the corresponding dielectric layer. The dielectric bumps in Lien (see the bumps intermediate between elements 224, 225, and 226 of FIG 3), do not qualify as support structures because the recited support structures overlie the bond pad. Nor is there any suggestion or motivation found with Freeman to connect support structures

to the un-removed portions of the corresponding dielectric layer because Freeman is not directed to providing mechanical support and protecting, against probe forces. Freeman is motivated by a desire to achieve greater planarity to facilitate bond pad photolithography processing. Because the free standing dielectric perforations accomplish that goal, Freeman does not suggest or motivate a modification to connect the structures to the un-removed portions of the dielectric. Accordingly, Appellants would respectfully submit that a prima facie case of obviousness has not been established for the claims in Group B.

Additional Arguments for Group C

In addition to the reasons presented above, Appellants believe the claims of Group C are not obvious over the cited references. The Group C claims include the formation of a barrier layer between the layers of the composite bond pad structure. The cited references fail to disclose or suggest this modification of Freeman because Freeman suggests a multi-layer bond pad in which all layers of the bond pad are comprised of the same or similar material. More specifically, Freeman makes the clear suggestion that all of its metal layers are the same. At column 3, lines 37-41, Freeman indicates that “first metal layer 13 is representative of all metal layers 18, 23, 27 in thickness, composition, method of deposition, and method of patterning.” Although Freeman indicates that the first metal 13 could comprise a material other than aluminum, there is no statement in Freeman suggesting the use of a first material for the first metal 13 and a different material for the subsequent metal layers. Freeman contains no such suggestion because layers of different composition are contrary to the formation of a uniform bond pad structure. In other words, Freeman is concerned with a method of planarizing a (typically) aluminum bond pad. As such Freeman contains no suggestion motivating multiple layers of different composition and contains a clear suggestion to the contrary that each layer of the bond pad is the same material. Lien does not even disclose a multi-layer bond pad structure. Because Freeman suggests each of its bond pad metal layers is the same composition, there is no need to

incorporate an intermediate barrier film and, to the contrary, doing so would only introduce additional processing steps. Accordingly, Appellants submit that a prima facie case of obviousness has not been established with respect to the Group C claims because there is lacking any suggestion or motivation to combine the cited references.

Arguments for Group D

In addition to the reasons presented above, Appellants believe the claim of Group D is not obvious over the cited references. The Group D claim specifically recites the formation of a composite bond pad structure in which a copper bond pad is capped by an aluminum capping layer with a barrier layer intermediate between the copper and the aluminum. Claim 30 stands rejected under Freeman and Lien although Appellants would submit that, because claim 30 is dependent upon a claim that was rejected under Freeman, Lien, and White, the Examiner intended to include claim 30 in the same ground of rejection as its parent. Even if the Examiner had cited White in the rejection of claim 30, however, the cited references fail to disclose or suggest the claimed limitations because, once again, Freeman suggests a multi-layer bond pad in which all layers of the bond pad are comprised of the same or similar material. As indicated above, Freeman makes the clear suggestion that all of its metal layers are the same composition. Although Freeman indicates that the first metal 13 could comprise a material other than aluminum, there is no statement in Freeman suggesting the use of a first material for the first metal 13 and a different material for the subsequent metal layers. Freeman contains no such suggestion because the preferred embodiment of Freeman discloses a bond pad comprised of multiple layers of aluminum. Since aluminum is a self-passivating metal, there is no need to cap the aluminum with another material because aluminum suffices as an upper, exposed layer for the bond pad structure. In contrast claim 30 recites a copper-barrier-aluminum bond pad structure incorporating a passivation layer that has been patterned to define support structures. Accordingly, Appellants submit that a prima facie case of obviousness has not been established with respect to the Group

D claim because there is lacking any suggestion or motivation to combine the cited references.

Respectfully submitted,

A handwritten signature in black ink, appearing to be 'J. Lally', written over the printed name.

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APPENDIX

1. A method of forming a semiconductor device, comprising:
 - forming a first interconnect level over a semiconductor substrate;
 - forming an uppermost interconnect level that includes an interconnect portion and a bond pad over the first interconnect level, wherein:
 - the interconnect portion contacts the first interconnect level by way of vias through an interlevel dielectric layer, and
 - wherein all vias interconnecting the interconnect portion and the first interconnect level are positioned outside regions directly below the bond pad;
 - forming a passivation layer over the uppermost interconnect level;
 - removing portions of the passivation layer, wherein removing portions of the passivation layer exposes portions of the bond pad and forms a plurality of support structures overlying the uppermost surface of the bond pad; and
 - forming a conductive capping layer overlying the plurality of support structures, wherein the conductive capping layer electrically contacts the bond pad.
2. The method of claim 1, wherein a copper content of uppermost interconnect level is at least 90 atomic percent.
3. The method of claim 1, further comprising forming dielectric studs within the bond pad, wherein at least a portion of a support structure overlies a portion of a dielectric stud.

4. The method of claim 1, wherein the dielectric layer includes a material selected from a group consisting of a nitrogen, a hydrogen, and a carbon containing silicon oxide.
5. The method of claim 1, wherein the plurality of support structures are interconnected with unremoved portions of the passivation layer.
6. The method of claim 5, wherein forming the uppermost interconnect level further comprises forming the bond pad over at least one dielectric layer having a Young's modulus less than approximately 50 Giga Pascals.
8. The method of claim 1, further comprising forming a barrier layer between the capping layer and the bond pad, wherein the barrier layer overlies the support structures and abuts exposed portions of the bond pad.
9. The method of claim 8, wherein the barrier layer includes a material selected from a group consisting of tantalum, titanium, tungsten, and chromium.
10. The method of claim 1, wherein the conductive capping layer includes aluminum.
11. The method of claim 1, wherein the conductive capping layer includes a material selected from the group consisting of nickel and palladium.
24. A method of forming a semiconductor device, comprising:
depositing a dielectric layer over a semiconductor substrate;

patterning and etching a trench opening within the dielectric layer;
depositing a copper layer over the dielectric layer and within the
trench opening;
removing portions of the copper layer not contained within the trench
opening to define an uppermost interconnect level comprising a
copper bond pad and an interconnect portion, wherein the
interconnect portion physically couples to an underlying
interconnect level by way of vias, wherein the vias are
positioned beyond regions directly below the copper bond pad;
forming a passivation layer over the uppermost copper bond pad;
patterning and etching the passivation layer to define openings and
support structures overlying the uppermost copper bond pad;
depositing a conductive layer over the support structures and within
the openings, wherein the conductive layer electrically contacts
the uppermost copper bond pad;
patterning and etching the conductive layer to define a capping film
over the support structures and the openings.

25. The method of claim 24, further comprising dielectric studs disposed within the uppermost copper bond pad, wherein at least a part of a support structure overlies a dielectric stud.
26. The method of claim 24, wherein the passivation layer includes a material selected from a group consisting of nitrogen-containing silicon oxide, a hydrogen containing silicon oxide, and a carbon containing silicon oxide.
27. The method of claim 24, wherein at least one of the support structures is interconnected with unremoved portions of the passivation layer.

28. The method of claim 24, further comprising forming a barrier layer overlying the support structures and within the openings prior to forming the conductive layer, wherein the barrier layer electrically contacts the uppermost copper bond pad.
29. The method of claim 28, wherein the barrier layer is further characterized as a tantalum barrier layer.
30. The method of claim 29, wherein the conductive film is further characterized as an aluminum film.
31. The method of claim 28, wherein the barrier layer includes a material selected from a group consisting of titanium, chromium, tantalum nitride, titanium nitride, and chromium nitride,
32. A method of forming a semiconductor device, comprising:
forming an uppermost interconnect level over a semiconductor substrate, wherein the uppermost interconnect level includes an interconnect portion and a bond pad, wherein the bond pad has dielectric studs disposed within the bond pad;
forming a passivation layer over the uppermost interconnect level;
removing portions of the passivation layer, wherein removing portions of the passivation layer exposes portions of the bond pad and forms a plurality of support structures overlying the uppermost surface of the bond pad, wherein at least a portion of a support structure overlies a portion of a dielectric stud; and
forming a conductive capping layer overlying the plurality of support structures, wherein the conductive capping layer electrically contacts the bond pad.